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Experimental evaluation on the silicon mechanical performance of electronic packaging

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ABSTRACT

Semiconductor packaging is trending towards a miniaturisation in size but an increase in functionality. Hence, the thickness of the silicon wafer has decreased dramatically with a concern on the possible degradation of the strength of the thinned wafer. In this paper, 3-point bend (3PB) on bare silicon is selected as the preferred silicon break strength (SBS) test methodology due to its setup effectiveness and subsequent application in the prediction study. This experimental testing study focused on evaluating the SBS from different thickness ranges. The study was then followed by evaluating the influence of a possible impact from flaw creation with laser marking on silicon surfaces. The results show that the SBS is consistent although with significant differences in the silicon thickness ranges. It is also revealed that the onset breaking load may not be a suitable metric and could be over sensitive on gauging the SBS comparison. The flaw creation from the engraving process revealed a significant drop of 75% SBS although with an approximate depth removal of <10% from the total thickness. The consistence failure mode is clearly visible and this left the silicon very vulnerable to catastrophic failure. This indicates that extra care is needed on ultra-thin silicon during the assembly process as fractures may happen even before any reliability stress test is conducted. Furthermore, the completion of the package level 3PB failure mode verification has helped to demonstrate that an SBS study can be conducted with a simplified bare silicon level testing. In short, the study with this simplified 3PB has successfully proven its usefulness in SBS estimation. The observed ultra-thin silicon SBS has degraded and strongly depended on the critical flaws especially from the surface defect and impact from the assembly handling.

Keywords: Semiconductor package; silicon break strength; 3-point bend; reliability; mechanical performance; laser marking.

INTRODUCTION

A semiconductor package is getting smaller in size but increases in functionality and performance requirement. Thus, this increases the risk on handling the ultra-thin silicon assembled on the electronic packaging [1-4]. High reliability performance remains an important necessity element; it requires a comprehensive understanding to appropriately characterise the possible strength of silicon and also the critical factors impacting its mechanical integrity [5] [6]. Silicon strength is normally evaluated with various lab scale bend or loading tests. There are many newly redefined testing methodologies and analysis approaches for the material strength study which include 3PB [7-11], four point bending (4PB) [12-14], ball/ ring on ring [15-17] and others that offer different advantages. In

general, the 3PB approach will result with an SBS range similar to the 4PB [12-14]. However, 4PB requires a more detailed test setup and also a relatively more complex analysis formulation. Lately, although indentation and scratch studies have been getting more popular on creating the potential controlled silicon defects, there are still limitations to be found with respect to a direct application on the immediate conversion of the SBS limit study compared to 3PB or 4PB. The 4PB was used as a more conservative measure of silicon strength for the design criteria [12], but with a more complex data analysis as compared to 3PB [13, 14]. Recently, an improved 4PB application has been developed by combining with the indentation test; nevertheless, this does not simplify the application of the 4PB test [18, 19]. Even though higher strength is estimated with the ball or ring related tests from the recent trend of literatures, it is suggested that those ball on ring (BoR), ring on ring (RoR) and ball breaker (BB) tests are only good in evaluating the silicon surface related strength, either without influence from the assembly process or with an intended focus on the potential treatment improvement on the silicon surface [12, 15-17, 20-24]. The critical impact, such as edge flaw or chipping, is excluded due to the nature of the test setup.

The overview of the 3PB test setup is shown in Figure 1 [7]. The test fixture is designed where the two bottom points are situated to provide support for the specimen, which incorporates a guided loading head to form a "3-point support and loading". Typically, the strength on the backside condition of the die is evaluated in this three-point bend test. The resulting bending moment is the highest at the centre of the backside. The region of this effect area with the highest stress is primarily at the centre region of the die backside surface, which also includes a minimal portion of the die edge. Thus, the die strength measured from this method is highly sensitive to the largest defects that are concentrated to the centre region on the backside; these may primarily be the damages caused by the wafer thinning processes, edge chipping or engraving effect.

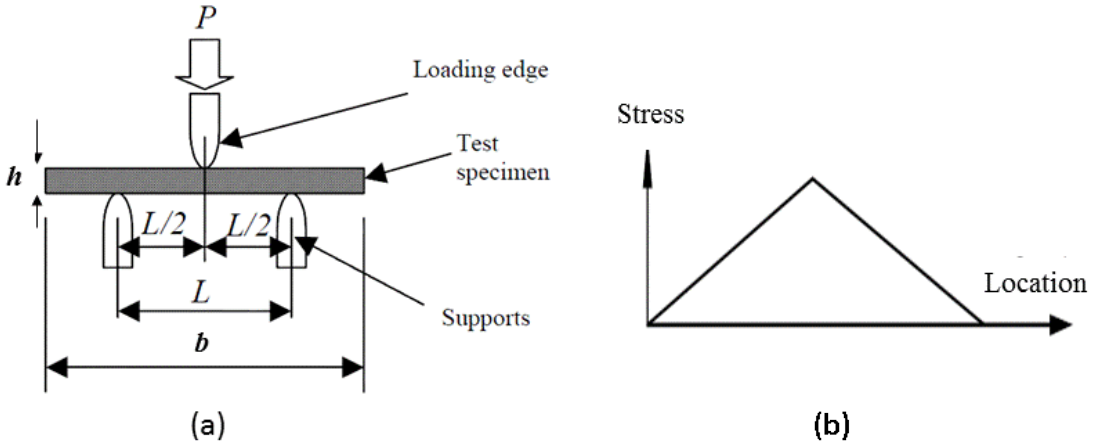

Figure 1. (a) 3PB test configuration and its reference parameters, (b) 3PB test loading characteristic and bending moment [7].

As illustrated in Eq.(1), the projected stress from the three-point bend test is calculated from the beam bending equation. The applied force at break (P_B, in Newton), the support span (L, in millimetre), the width of the test specimen (b, in millimetre) and the thickness of the specimen (h, in millimetre) will be calculated to estimate the flexure stress (σ_{fb}) of silicon with a linear stress/ strain behaviour. The detail setup is documented in various literatures [7-11, 17]. Jie-Hua et al. stated that 3PB is a simple test but it is modified from a method used to measure the strength of brittle materials, such as ceramics

[15]. Besides, the strength measured from this method is highly sensitive to the largest defects that are closest to the centreline on the backside, namely the damage caused by the wafer thinning processes, which was observed by [12]. Also, Werner et al. stated that the minimum radius a chip can reach before it cracks is the parameter used to characterise the flexibility of this chip [22]. Hence, it is not surprising that this 3PB method is simple and good enough to evaluate the silicon strength with inclusion of both thinning (die surface defect) and singulation processes (edge chipping).

$$\sigma_{3PB} = 3\mathrm{PL}/2bh^2 \tag{1}$$

Also, in order to estimate and compare the stress from the bending of the silicon, a reference to Stoney's formula, Eq.(2) is employed too [25]. This equation is, in general, used for calculating the stress of thin films. Although the damaged layer is not a real thin film, it is assumed as a thin layer and its stress can be calculated, where $E / (1 - v)$ is the biaxial modulus of the substrate, h is the substrate thickness, t is the film thickness, and R is the radius of the curvature. This analytical estimation will be compared to the experimental data to check on the sensitivity of the available lab scale test data, which is also being explored by [26], before analysing the bending stress from the curvature of a silicon wafer.

$$\sigma = \frac{\frac{E}{1-v}h^2}{6Rt} \tag{2}$$

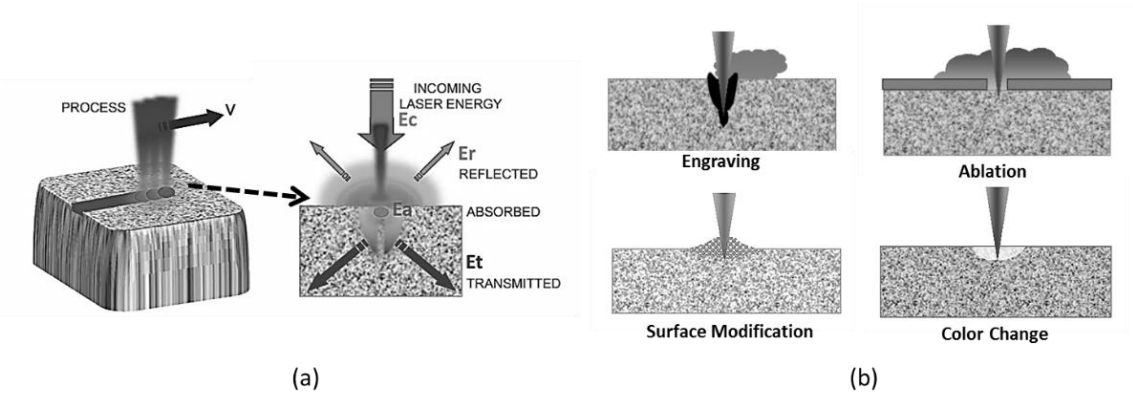

Figure 2. (a) Illustration of how a laser works on a designated material and (b) Various types of laser marking techniques on a silicon surface for the electronic industry shared by [27].

The SBS study in this paper also includes the influence of the possible impact from flaw creation, such as laser marking on silicon surfaces. The laser marking of silicon has been an important standard for many years especially in the solar cell industry [28]. It provides a good traceability along the entire value chain and over the whole lifetime with a hard physical coding, which has also been heavily adopted for electronic packaging's silicon marking [27, 29]. As illustrated in Figure 2(a), the "marking" is realised by the portion of the laser radiation absorbed by the material. Lately, there are various types of laser marking techniques, commonly named engraving, ablation, surface modification and colour change, which are shown in Figure 2b. There are several researchers studying the effect of laser marking on the silicon. Gu [30] initially conducted a study on laser marking on a chip scale package. The effort was further explored to

investigate various marking parameters and options for good manufacturability in solar panels. However, the study is more on the physical attributes of silicon, such as the wear and tear, breaking point and fatigue failure [28, 31]. The impact of laser marking on the silicon strengths is hardly discussed, thus it is identified as a possible impactful factor on a controlled flaw creation to be further investigated in this paper.

A refined 3PB bend test and its applicability to the silicon failure strength will be evaluated in this paper. The data analysis simplicity however does not impact its test output and quality without a need of complicated sample preparation and test setup. Besides, the overall SBS database from this study will be compared to the available literatures' findings mainly to evaluate its metrology robustness and also as a quick benchmark between the selected 3PB with different SBS techniques. Additionally, the important study on the influence of the laser marking process on the SBS is also included. This unexpected but crucial impact factor is limited in existing literatures especially with detailed observation of its engraved depth to the SBS performance. This process causes an unpredicted stress concentration which easily reduces the SBS when subjected to the 3PB test. The failure analysis with the combination of destructive and non-destructive approaches will also be discussed in detail to establish the failure mode verification between stand-alone silicon and a fully assembled package.

METHODS AND MATERIALS

Design of Experiment

Dummy wafers were selected as test vehicles to characterise the apparent die strength. The advantages of using dummy wafers are the ease of wafer sources and custom-designed die configuration. The test sample is with an isotropic behaviour of silicon in the <100> plane. The present study aims to use the 3PB approach to establish a wide range of SBS on various ultra-thinned silicon within the range of <1.0mm. The samples were ground and diced to the required size and thickness before being subjected to the test to record its onset failure load. The detailed coverage of various thickness values is as documented in Table 1. The data was analysed using Eq. (1) to estimate the ultimate failure stress upon silicon breakage as the measure of SBS.

Table 1. Various test specimen preparations for the thickness impact study.

Sample Preparation	Thickness (μm)	Data Collection & Analysis
Various thicknesses from Grind, Dice and Lapping	Various and <1mm	Breaking force (SBS estimation) & failure mode (defect depth)

Table 2. Various evaluation parameters for the test specimen preparation.

Sample	Laser Marking Type & Setting	Data Collection and Analysis
Designated Thickness	Engrave Marking (No Mark/ Notch Mark/ Groove Mark) & Nominal Notch Mark Power / +25%/ +50%	Breaking force (SBS estimation) & failure mode (defect depth)

As mentioned in the previous section, there are some unintended flaw-creations along with the engraving laser in the manufacturing process. This unexpected engraved

"defect" causes multiple stress concentration points, which will easily reduce the SBS when subjected to any mechanical or handling stress. Hence, this premeditated laser marking impact is characterised in detail in this paper, where different test sample preparations are included in Table 2.

Experimental Procedure

As shown in Figure 3, an MTS series of universal testing machines with a 100N load cell was used to conduct a lab scale table top 3PB test for SBS data collection [32]. The load cell accuracy is ±1% of the indicated test force range of interest in this paper. To derive the Eq. (1) for the bending stress in the current study, the following assumptions of small deflection and pure bending stress were made. The tip of the loading edge and supports were hardened to avoid any unexpected deformation during the test. The loading speed was set to be equal or less than 5mm/min in order to avoid any impact event or noises on the test specimen as documented in [7]. About 25 test specimens per each thickness were prepared, which were picked from different wafer locations. The breaking force of test specimen with different thicknesses was recorded where variation was expected depending on the silicon thickness. The SBS ratios were computed by comparing to the maximum SBS established with available literature test data. The failure analysis was also conducted after the 3PB test in order to differentiate the potential failure modes. The post marked depth on a silicon surface is another important comparison data for assessing its influence on SBS. Similar to the surface roughness, the mark depth measurement can be obtained with a non-contact methodology such as utilising microscopy for the three dimensional surface profile. This technique shows that the engraved depth can be studied even with a single full field view capability. Alternatively, a conventional cross-section with an SEM zoom-in view approach can also be accomplished. However, since this is a destructive approach, the method will only be applied once the full test study has been conducted. This paper also demonstrates the combination of the previously discussed methods to gather the useful mark depth information, the results of which will be discussed in detail in the next section.

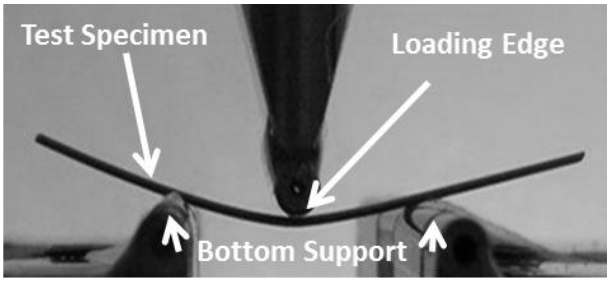

Figure 3. Lab scale 3PB setup on the test tool with a loading edge that was held by two bottom supports.

RESULTS AND DISCUSSION

Influence of Silicon Thicknesses on SBS

An investigation on silicon strength with 3PB was conducted with various silicon thickness values. The comparison on this various silicon thicknesses and respective broken forces is shown in Figure 4a. The result shows an increasing trend of the silicon breaking load with die thickness. This is expected as a larger load is needed to cause

breakage in silicon with a greater volume, as reported by [10, 33]. However, the strength of silicon should not be measured using breaking force or load, since it is not representing the generic material characteristic property of the silicon. This may be valid as a fair comparison if only comparing different skews of the test specimen with same thickness [34]. Hence, although the silicon broken force decreases in proportion to the chip thickness, the silicon breaking strength (SBS) may vary due to its position within a wafer as well the grinding process, but it is expected to be in a constant range regardless of the chip thickness [33]. By applying Eq.(1), the flexure stress (σ_{fb}) at the breakage of the silicon specimen can be estimated correctly. This eventually suggests that SBS is ranging between 0.2 and 0.6, as illustrated in Figure 4b. Also, this SBS range with such die thicknesses was within the variations that were estimated from [9-11, 19, 35, 36]. The differences could be due to the discrepancy of the sample preparation, different silicon type and with the combination of 4PB and those ball ring tests setup [12, 15-17, 20-23]. However, a slight improvement at a lower thickness value was observed; this may be attributed to the extra removal of silicon defects and damage layers during the thinning and surface treatment processes. A clear increasing trend in the breaking load was noted but not the breaking stress or strength. From these force and strength findings, it is clearly implied that processing a thin silicon specimen requires a great deal of expense and energy. This is mainly due to the silicon becoming incredibly fragile at this range of thickness, in which fractures may occur within a deflection of 1 mm [37]. The results show that the SBS is the optimum and stable metric although with significant differences in the silicon thickness ranges. This also revealed that the onset breaking load may not be a suitable metric and could be over sensitive to gauging the SBS comparison. However, this also indicates that the build-up stresses on the silicon surface may be similar when trending to ranges lower than 1 mm; a low bending force from any manufacturing process could be sufficient to cause a catastrophic silicon failure.

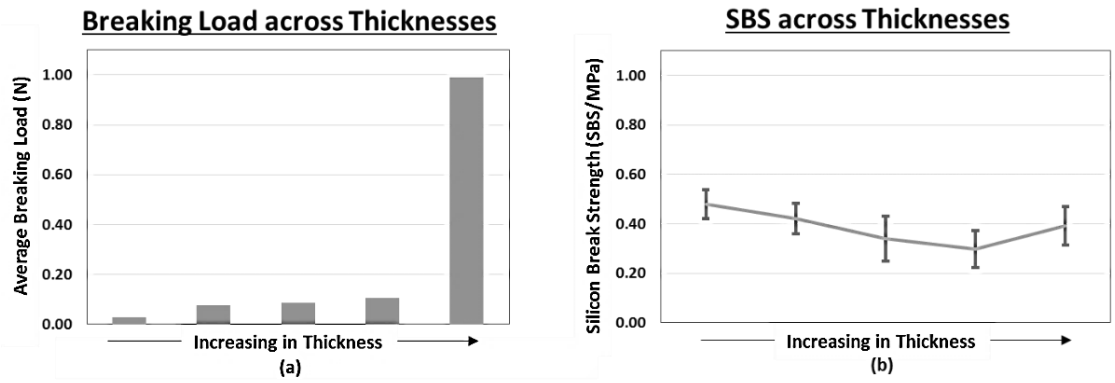

Figure 4. **(**a) Significant variation in the breaking force ratio but (b) observed a constant SBS range across different thickness values within a 1 mm range.

This lab scale result is further compared to the analytical approach with Stoney's formula. By applying the bending displacement data from Figure 5a into Eq.(2), the two 3PB and Stoney's results are in similar trends, which may be attributed to the same assumption aligned to the beam bending theory. However, as shown in Figure 5b, the differences in the estimation differences may be attributed to a 3PB bending moment that is not aligned with the crucial assumption of Stoney's formula, where film stresses and the associated system curvatures are non-uniformly distributed over the test specimen

area [38]. Moreover, the variations of the silicon thickness on the displacement loading and micro-defect on the actual silicon surfaces may also contribute to the potential differences [26]. Hence, the appropriate SBS estimation of a silicon should be accomplished with a lab scale test but Stoney's formula can be utilised for a thin film stress for a possible wafer warpage stress. Those bending stresses are mostly developed through a defined system curvature with a wafer bowing effect.

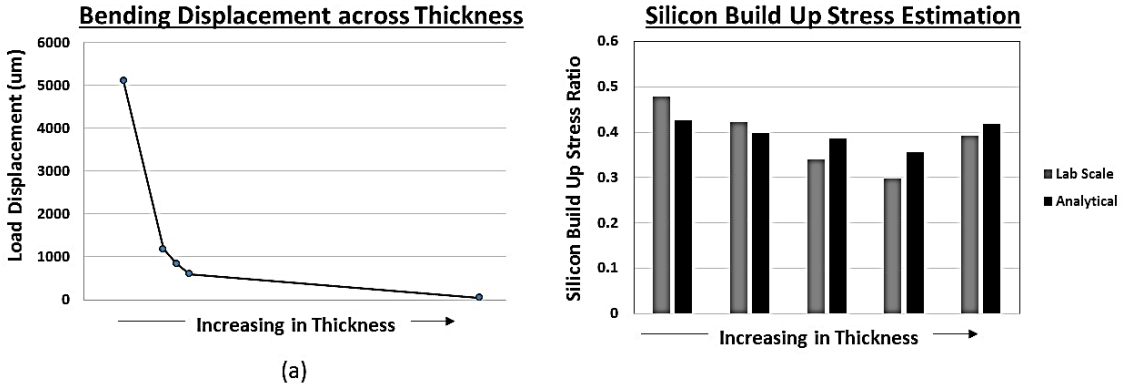

Figure 5. (a) Bending displacement plot with various silicon thickness values and (b) Comparison between the lab scale tests (3PB) and the analytical analysis with Stoney's Formula.

Table 4: Summary of the estimated silicon strength limits with different approaches

Approach/ Method	Strength estimation ratio range	Discussion
3PB (Existing Paper)	0.30 - 0.58	Still the preferred test method due to its cost and time effectiveness with a similar range of average responses from [10-12, 15, 17, 19, 22, 36, 37].
4PB	0.20 - 0.58	4PB has a close approximate to 3PB but requires a more detailed test setup as pointed by [12-14].
Nano-Indentation/ Scratch	0.20 - 0.25	Requires careful data interpretation. Some literatures suggested a >1.0 ratio range but disclosed an unclear analysis approach [18, 24] [18 & 24].
RoR/ BoR/ BB	0.42 - 1.00	Higher strength is expected with extra treatment on the silicon surface without major influence of edge defects or chipoff [12, 15-17, 20-23].

In general, the 3PB approach provides results in the SBS range similar to other test methodologies. The possible influence of impurities and micro-defects on the actual silicon surfaces on different test specimens may contribute to the potential differences estimated from different methodologies or setups. Nonetheless, the 3PB bend is still the preferred test methodology due to its cost and time effectiveness. It also brought many advantages in terms of setup and data interpretation simplicity. The comparison between various test methodologies' strength range and applications from different literatures on the estimated SBS is summarised in Table 3 for ease of reference.

Influence of the Silicon Marking Process

A significant drop of 75% SBS is clearly visible when a marking was engraved on the silicon surface, as shown in Figure 6a. This engrave marking, with either notch or a groove type, involved silicon removal from the silicon surface, which caused significant stress concentration during the bend test loading (tensile stress). Therefore, the marking constituting either a scratch or carving on a smooth silicon surface, eventually reduces the SBS that causes significant silicon failure (silicon crack). It increases the propensity to cause the silicon performance loss due to cell cracking as observed by [39]. Also, the lack of scatter in the data plot in Figure 6 for both the groove and notch marking solutions suggests that they fail with almost consistent breaking mode, which will be discussed in the subsequent section. The further study on the increment of laser power in notch marking (+25% & +50%) during the engraving process also revealed that it further weakened the SBS by approximately 30%. The observation is shown in Figure 6b and it indicates that the higher power of laser marking results in a deeper mark depth which could eventually lower the SBS to below that of the 0.10 ratio region. The improper laser grooving process had eventually caused many dies broke during the pick-up process in the dicing technique study as well [40]. Also, a non-optimised marking solution is too risky since it over-reduces the SBS of the silicon at the assembly even lower than the possible strength limit prior to any reliability stresses. This effect is crucial and may cause a catastrophic failure at the assembly process since silicon marking is required as part of the component traceability which required significant characterisation work for ultra-thin silicon.

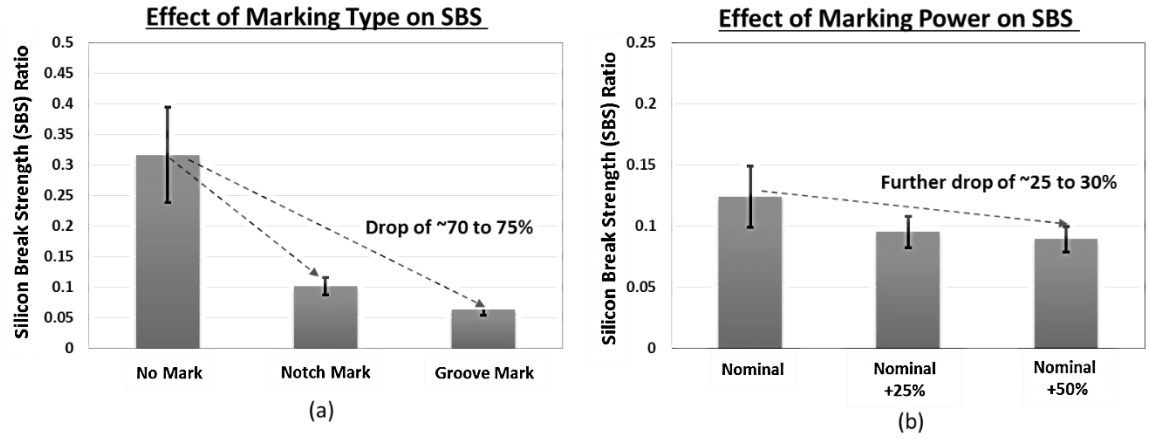

Figure 6. (a) SBS comparison on different marking processes. (b) Influence of marking power with notch marking on SBS.

Failure Mode Investigation

Failure is more severe for samples where surface or edge damage is prevalent. Such kind of silicon tends to fracture with fewer broken pieces, as shown in Figure 7a. This manner of fracture is an indication of lower SBS, as depicted in Figure 4. The stresses are easily concentrated on the silicon surfaces irregularities, such as edge chipping, indent points or engraved mark to propagate and eventually form a full crack. On the other hand, samples with reduced defects, such as good surface polishing as well as those without any pre-marking are significantly stronger. Fracture in these samples is characterised by shattering, as shown in Figure 7b, at the time of failure due to the elastic energy being released when the fracture starts. The package level 3PB verification has also successfully demonstrated that a SBS study can be conducted with a simplified silicon level testing, with a similar failure mode as shown in Figure 7c. This significantly helps the SBS

evaluation, without a need to prepare a fully assembled test sample, but still replicates a similar stress state at the final product assembly condition. The discovery is also important in aligning towards package level silicon stress prediction and sensitivity study that can be estimated with a modelling approach, compared with the established SBS limit. These failure mode findings are aligned to the proposed systematic flow implemented in the existing study for silicon crack modes, which are seldom documented in literatures for good benchmarking.

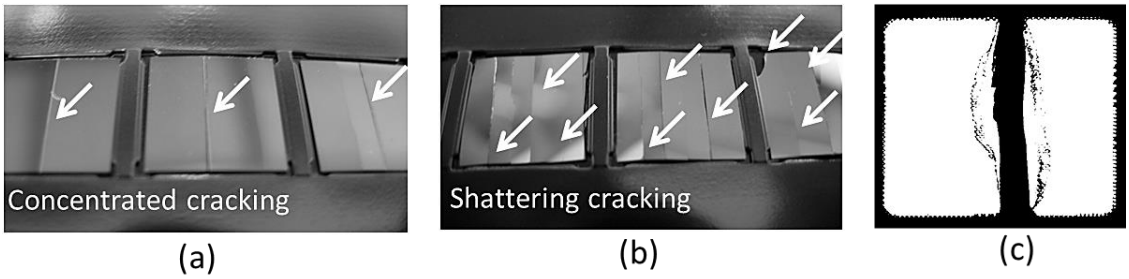

Figure 7. Different breaking modes observed on (a) a type of notch/ groove laser marking compared to (b) with no mark silicon on the silicon level test. (c) CSAM verification on the package level failure mode.

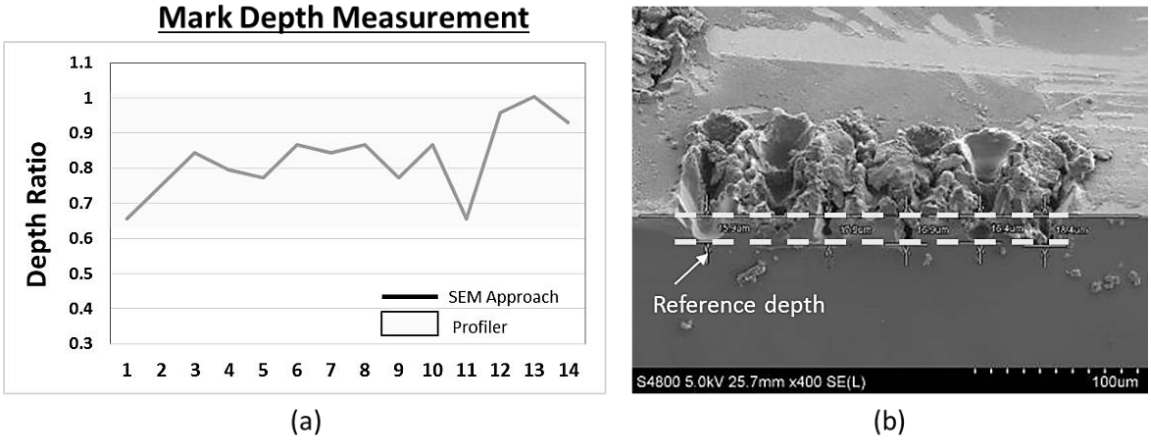

Figure 8. (a) Comparison of the measurement depth ratio of a laser marked area using the SEM approach and non-contact surface profiler. (b) Example of the reference location for measurements.

Additional characterisation data were collected on the laser engraved samples as shown in Figure 8 on both physical cross sections with a non-contact method, respectively [41]. The result revealed that both approaches detected comparable mark depths, ranging between 0.7 and 1.0 depth ratios. The potential slight difference on the cross section was maybe due to the extra errors dealing with the tilting of reference plane during the depth measurement step. Hence, the combination of both destructive and non-contact methodologies provide good selection for the user to extract a practical data set for reference since the SEM cross section is a destructive approach and barely able to recover the processed samples.

CONCLUSIONS

In this study, the silicon strength, evaluated with a redefined 3PB, has successfully proven its usefulness in the SBS estimation along with its simplicity. The results show that the SBS is the optimum and stable metric although with a significant reduction of silicon thickness estimated below the 1 mm range. This also revealed that the onset breaking load may not be a suitable metric and could be over sensitive on gauging the SBS comparison. This 3PB approach on SBS across different thickness values showed a good proximity and produced the SBS range similar to other types of complex test methodologies. However, this also indicates that the build-up stresses on the silicon surface may be similar when trending to the ultra-thin thickness range; a low bending force from any manufacturing process could be sufficient to cause a catastrophic silicon failure. Besides, the appropriate SBS estimation of a silicon should be accomplished with a lab scale test, whereas Stoney's formula is more suitable for a thin film stress for a possible wafer warpage stress study. The follow-up investigation on the laser marking solution revealed a significant margin reduction, recorded as high as 75% on average. In addition, the higher power of laser marking was used for deeper mark depth, which eventually caused the SBS to dip even below the sub 0.1 ratio region. This is a crucial finding, which had been hardly evaluated in the past when the marking was initially introduced to provide for product lifelong traceability. The follow-up failure mode study also demonstrated a systematic characterisation and FA flow implemented with and without destructive methods in the existing silicon crack study. Both approaches have demonstrated a small delta (<5%) in measurement differences, which provides a good selection for users to extract a practical data set for reference before conducting a further destructive evaluation. Also, the package level 3PB verification has successfully demonstrated that a SBS study can be conducted with a simplified silicon level testing. In summary, besides the contribution from different test approaches, the observed SBS levels strongly depend on a few critical parameters, which include the relative probabilities of edge and surface flaws, the surface treatments and assembly handling. This experimental discovery highlights a potential need to have a more synchronised experimental study with the use of a modelling analysis for good cross database leveraging and prediction. The finite element analysis (FEA) could be employed to drive the team for the next possible focus on exploring the parametric modelling study on the silicon surface build-up stress investigation on a microsystem.

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